Characteristics of Deep-Submicrometer MOSFET and Its Empirical Nonlinear RF Model

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***Abstract*—Si MOSFET's with submicrometer gate length were fabricated and characterized by RF evaluation. Devices with a 0.25-μm gate length demonstrated a g_m of 258 mS/mm, an f_T of 28 GHz, and a minimum noise figure of 1.8 dB at 900 MHz. A nonlinear device model was constructed based on the measured results. Empirical equations are used to represent the nonlinear elements such as g_m, $C_{\rm gs}$, $C_{\rm gd}$, $C_{\rm ds}$, and $R_{\rm out}$. These nonlinear elements, together with device parasitics, provide designers with a comprehensive model for using these devices for RF circuits.**

***Index Terms*—Empirical RF model, microwave characteristics, MOSFET.**

I. Introduction

RECENT advances in Si MOSFET's with a submicrometer gate length have made these devices an attractive candidate for RF designers to implement in microwave circuits [1]–[3]. Since the manufacturing maturity of Si integrated circuit (IC) technology is well established and is much better than the technology developed for GaAs, Si RF IC's and, therefore, plays a major role for wireless communication operated below 2 GHz. In order to ensure the circuit performance for the required frequency bands and also shorten the design cycle, device models are very critical [4]–[7]. Also, a well-described nonlinear device model is crucial for large-signal or harmonic operation. This model should take into account parasitic effects which are serious at high-frequency operation. In addition, a comprehensive model should also take care of the nonlinear elements where these elements are sensitive to bias conditions.

In this study, we characterized the dc and RF performance of the recently developed advanced Si MOSFET's for mass production with a minimum gate length of 0.25 μm. As for the MOSFET model, we first evaluated device high-frequency parasitics, and since the RF model is hard to be realized by physical formula, we used purely empirical equations to describe these nonlinear behaviors. The fitting parameters in these equations are determined by the measured results. By combining the parasitics and a nonlinear formula, MOSFET's with deep-submicrometer gate length can be fully characterized and implemented in RF circuit design.

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TABLE I
SUMMARIES OF dc AND RF PERFORMANCE OF n-MOSFET's WITH A GATE LENGTH OF 0.35, 0.3, AND 0.25 μm

Channel Length (μm)	0.35	0.30	0.25
V_{gs} (V)	2.1		
V_{ds} (V)	3.0		
$g_{m,peak}$ (mS/mm)	242	249	258
I_{ds} (mA)	34.5	44.7	40.7
f_T (GHz)	22.6	26.8	28.0
f_{max} (GHz)	12.0	12.5	15.0

II. Characteristics of Deep-Submicrometer MOSFET's

Si n-MOSFET's were processed by using advanced 0.25-μm technology on an 8-in wafer. The starting material was p-substrate (10-$\Omega\cdot$ cm). After shallow isolation trenches were formed, the well and channel implants were processed and the gate oxidation deposited. The peak doping concentration at the Si surface is about 2×10^{17} cm^{-3}. The physical gate–oxide thickness is 5.5 nm. After gate formation, lightly doped drain (LDD) implants were performed, followed by a nitride spacer. The source/drain region and gate poly were implanted at the same step forming n^+ and p^+ gates for n- and p-channels MOS, respectively. Subsequently, titanium silicide was formed on the source/drain gate poly. Tungsten plugs for contacts and metal interconnect consisting of Al–Cu and barrier metals were used. This 0.25-μm n-MOSFET shows a threshold voltage of 0.57 V and a saturation current of 6.27 mA (gatewidth $= 10$ μm).

To evaluate the gate-length-related device performance, MOSFET's with 0.35-, 0.30-, and 0.25-μm gates were all fabricated simultaneously by the same technology. Device dc *I–V* and *S*-parameter measurement were conducted by HP IC-CAP software in conjunction with a network analyzer, a dc source/monitor, and an RF probe station, and the results are listed in Table I. In order to be compatible with the RF probe, coplanar waveguide structures were used in devices for the final interconnecting metal layouts. The calibration of measurement system was done through the on-wafer (alumina substrate) open, short, through, and load patterns. Under the same bias condition, the peak extrinsic transconductance (g_m) systematically increased with shrinking gate length, from 242 mS/mm for 0.35 μm to 249 mS/mm for 0.3 μm, and to 258 mS/mm for 0.25 μm. This performance enhancement was also confirmed by RF evaluation, where f_T is increased from 22.6 to 26.8 GHz, and to 28 GHz. $f_{\rm max}$ is lower than f_T due to a higher gate resistance in submicrometer gate structures.

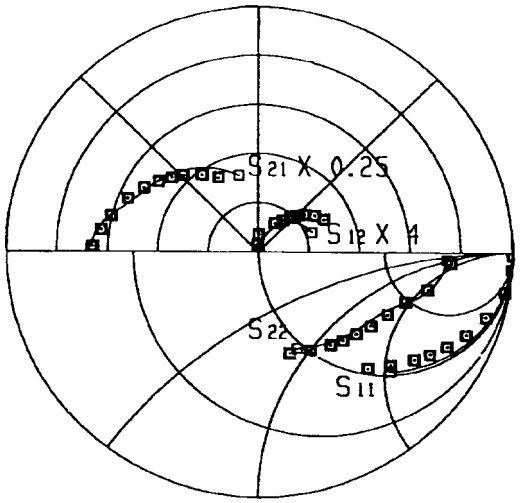

Fig. 1. Measured and simulated S-parameters of 0.25-μm n-MOSFET's. (frequencies: from 50 MHz to 6 GHz)

This will be confirmed by the following parameter extraction procedure.

The measured and modeled S-parameters of 0.25-μm MOSFET's are shown in Fig. 1, and Fig. 2 shows the equivalent circuit model. This model includes extrinsic elements which are bias independent, and intrinsic elements which will be affected by the bias conditions. In order to obtain the best fitting, $R_{\rm dd}$ and $C_{\rm dd}$ in series are needed in the drain end to model the substrate body effect, which is dependent on the substrate bias. Therefore, through the whole course of this study, we kept the substrate terminal grounded. Although this substrate bias dependence (so-called body effect) should also be modeled in the source, its effect there is usually not significant and can be ignored. These small-signal equivalent circuit parameters for MOSFET's biased at the same condition are listed in Table II. By shrinking the gate length (as seen from Table II), g_m increases and output resistance $(R_{\rm out})$ decreases. The decrease of $R_{\rm out}$ is resulting from the so-called short-channel effect, due to a strong electric field near the drain region. The gate resistance (R_g) was around 40 Ω, which is associated with gate resistivity and physical cross section, and lowers the $f_{\rm max}$ values. The typical gate resistance of 27 Ω (poly-gate) was obtained in our 0.6-μm gate-length MOSFET's. This 0.25-μm process used poly–silicide gate which, in principle, should provide a high thermal stability and a low resistance. However, the formation of silicide layer is relatively difficult to be completed in a deep-submicrometer region, which causes a higher resistivity. MOSFET's with a 0.3-μm gate length seem to perform better as far as the parasitic resistance, i.e., $R_g + R_s + R_d$, are concerned. The lower parasitic resistance also yields a lower device noise figure.

The device noise performance was evaluated by an on-wafer probe ATN system, with results summarized in Fig. 3. By varying $V_{\rm gs}$, a minimum noise figure of 2.5 dB at 1.8 GHz was obtained. These minimum noise figures are relatively insensitive to the gate length and bias conditions. However, the associated gain increased when the gate length decreased. As

TABLE II
SMALL-SIGNAL EQUIVALENT CIRCUIT PARAMETERS OF SUBMICROMETER MOSFET's, EXTRACTED FROM THE MEASURED S-PARAMETERS

Gate-Length / Parameters	0.35μm	0.30μm	0.25μm
V_{gs} (V)		2.1	
V_{ds} (V)		3.0	
I_{ds} (mA)	34.5	44.7	40.7
R_g (Ω)	40.7	38.1	43.6
R_d (Ω)	5.1	4.0	5.3
R_s (Ω)	1.1	0.85	1.2
L_g (pH)	2.7	1.8	2.5
L_d (pH)	2.3	1.5	1.9
L_s (pH)	1.7	0.83	1.0
C_{gd} (fF)	48.0	47.1	41.0
C_{gs} (fF)	245	226	208
C_{ds} (fF)	158	232	106
R_{out} (Ω)	409.9	299.7	183.9
C_{dd} (fF)	600	380	154
R_{dd} (Ω)	269.9	260.5	270.2
g_m (mS)	27.6	29.4	31.5

to the other operational frequencies, we observed a minimum noise figure of 1.8 dB at 900 MHz and 3.1 dB at 2.4 GHz. The noise parameters, which can be expressed by the following equation, are listed in Table III:

$$F = F_{\rm min} + \frac{4r_n|\Gamma_s - \Gamma_o|^2}{\left(1 - |\Gamma_s|^2\right)|1 + \Gamma_o|^2}. \tag{1}$$

A gate length of 0.3 μm achieved the lowest equivalent noise resistance (R_n), which corresponds to the lowest noise figure. If we examine the equivalent circuit parameters in Table II, we find that the MOSFET with a 0.3-μm gate length has lower R_g and R_s values, and these two elements have a strong influence on device noise figure. The optimum input-matching conditions to achieve the minimum noise figure for these three devices are more or less located in the same position.

III. NONLINEAR MODEL FOR DEEP-SUBMICROMETER MOSFETS

The traditional approach for Si MOSFET RF modeling is based on SPICE-related programs. In this case, both dc *I–V* and RF S-parameter should reach a fair agreement simultaneously with the measured results. However, as we can see in Fig. 2, in addition to the bias independent extrinsic elements, there exists some intrinsic elements such as g_m, $C_{\rm gs}$, $C_{\rm gd}$, $C_{\rm ds}$, and $R_{\rm out}$ that are influenced by both $V_{\rm ds}$ and $V_{\rm gs}$. These bias-dependent elements are very hard to be formulated by a physical equation, but the nonlinear behaviors of these elements are very important for RF circuit design. Therefore, we used purely empirical equations to represent these nonlinear elements. $V_{\rm ds}$ and $V_{\rm gs}$ are the two variables in these equations, and fitting parameters are determined by the measured bias-dependent S-parameters. These empirical equations can be fully adopted in the commercially available software for future circuit design.

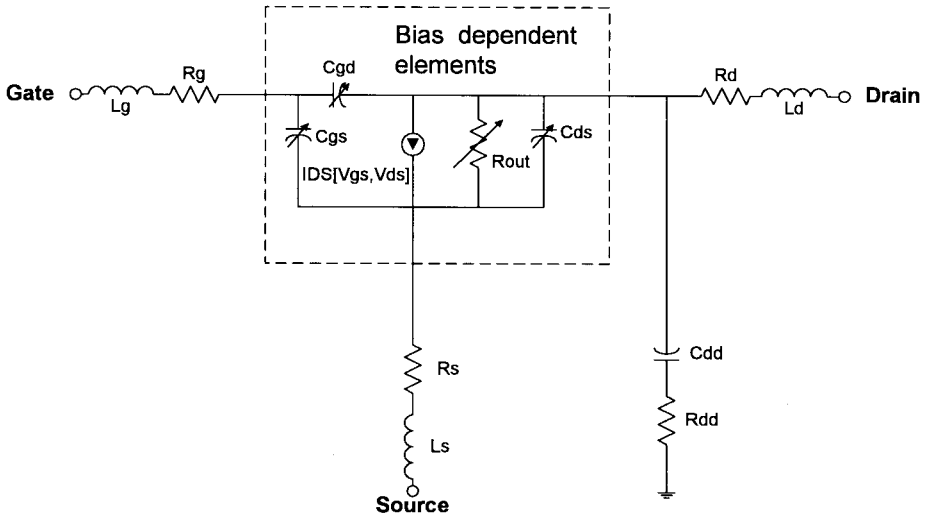

Fig. 2. Equivalent circuit model for submicrometer n-MOSFET's, including bias-dependent nonlinear elements.

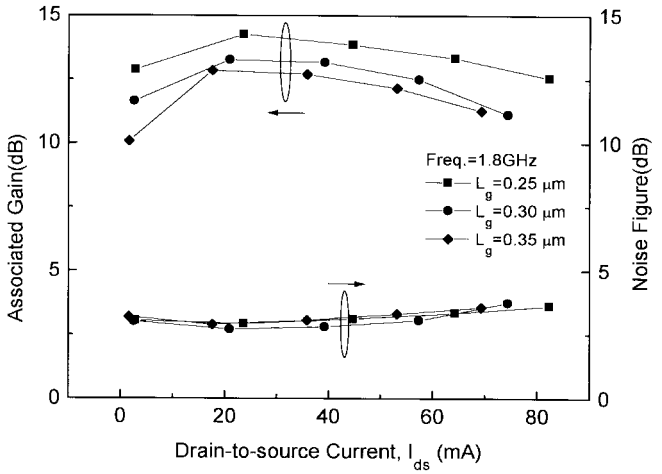

Fig. 3. Minimum noise figures and associated gains of submicrometer n-MOSFET's at 1.8 GHz.

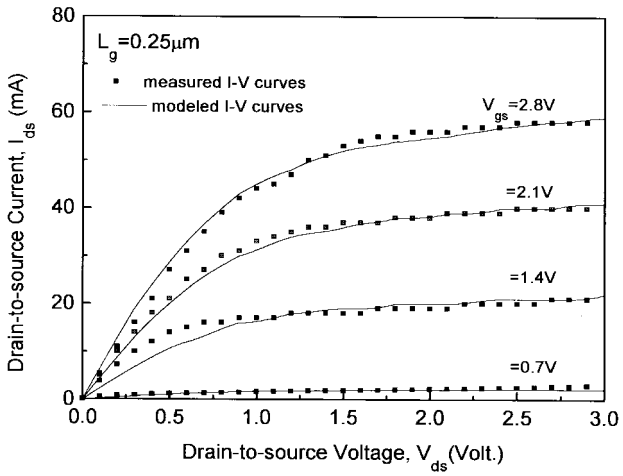

Fig. 4. Measured and modeled $I_{\rm ds}$–$V_{\rm ds}$ characteristics of 0.25-μm n-MOSFET's. The modeled results were obtained from (2), where $I_{\rm pk} = 35$ mA, $V_{\rm pk} = 2.2$ V, $\lambda = 0.074$, $\alpha = 1.3$, $P_1 = 0.5$, and $P_2 = 0.34$.

TABLE III
SUBMICROMETER n-MOSFET'S NOISE PARAMETERS AT 1.8 GHz

Channel Length (μm)	0.35	0.30	0.25
Frequency (GHz)	1.8		
V_{gs} (V)	1.4		
V_{ds} (V)	3.0		
I_{ds} (mA)	17.6	20.9	23.6
R_n (normailzed)	2.7	2.3	2.7
Γ_{opt} (mag.)	0.76	0.74	0.76
Γ_{opt} (ang.)	14.0	14.4	14.0
Gain (dB)	12.9	13.3	14.3
Fmin (dB)	2.7	2.5	2.9

Since the channel current $(I_{\rm ds})$ is dependent on $V_{\rm gs}$ and $V_{\rm ds}$, the nonlinear current source can be described by the following equation [8]:

$$I_{\rm ds} = I_{\rm pk}(1+\tanh(\psi))(1+\lambda V_{\rm ds})\tanh(\alpha V_{\rm ds})$$

where

$$\psi = P_1(V_{\rm gs} - V_{\rm pk}) + P_2(V_{\rm gs} - V_{\rm pk})^3 \qquad (2)$$

and $V_{\rm pk}$ is the $V_{\rm gs}$ at peak g_m position. Fig. 4 shows the measured and modeled *I–V* characteristics of a 0.25-μm MOSFET. It is seen that (2) can fully characterize nonlinear *I–V* characteristics.

Subsequently, a set of multibias S-parameters of 0.25-μm MOSFET's were measured by a network analyzer. A typical S-parameter was first chosen to obtain the best fitting according to the equivalent circuit model, shown in Fig. 2. Since the parasitic elements in this model are defined as bias independent, we kept these values as constants and only modified those bias-dependent elements for the other S-parameter fitting at the different bias conditions. Therefore, we can extract these nonlinear elements, namely $C_{\rm gs}(V_{\rm ds}, V_{\rm gs})$, $C_{\rm gd}(V_{\rm ds}, C_{\rm gs})$, $C_{\rm ds}(V_{\rm ds}, V_{\rm gs})$, and $R_{\rm out}(V_{\rm ds}, V_{\rm gs})$ based on the measured results. Then, combining with the previous *I–V* fitting, it concludes the establishment of empirical nonlinear RF MOSFET model.

The $\tanh(x)$ function is the most common fitting equation for these nonlinear behaviors [8]. The following equations are

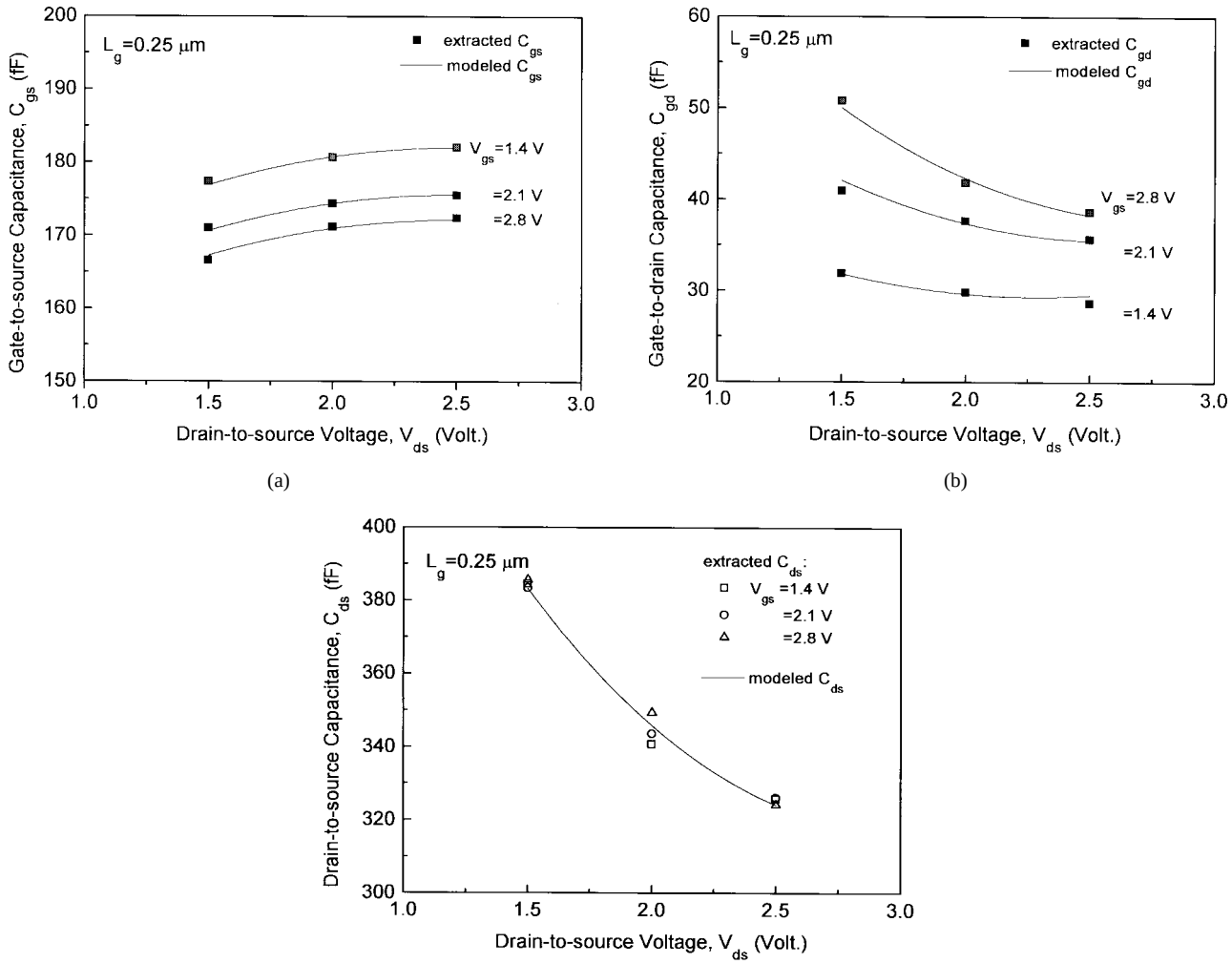

Fig. 5. Extracted and modeled bias dependent capacitances (a) $C_{\rm gs}$, (b) $C_{\rm gd}$, and (c) $C_{\rm ds}$. The modeled results were optimized by (3)–(5), respectively, where $C_{\rm gs0} = 105$ fF, $P_{\rm gs0} = 1$, $P_{\rm gs1} = 0.076$, $P_{\rm gs2} = -0.087$, $P_{\rm gs3} = 0.041$, $Q_{\rm gs0} = -0.25$, $Q_{\rm gs1} = 0.13$, $Q_{\rm gs2} = -0.028$, $Q_{\rm gs3} = 1.5 \times 10^{-4}$ in (3), and $C_{\rm gd0} = 201$ fF, $R_{\rm gd0} = 1.3$, $R_{\rm gd1} = -0.37$, $R_{\rm gd2} = -1.3$, $R_{\rm gd3} = 0.61$, $S_{\rm gd0} = 0.97$, $S_{\rm gd1} = 0.083$, $S_{\rm gd2} = 0.073$, $S_{\rm gd3} = 0.0028$, $S_{\rm gd4} = -0.013$ in (4), and $C_{\rm ds0} = 609$ fF, $T_{\rm ds0} = 0.34$, $T_{\rm ds1} = -0.57$ in (5).

used to get the best fitting for $C_{\rm gs}(V_{\rm ds}, V_{\rm gs})$, $C_{\rm gd}(V_{\rm ds}, C_{\rm gs})$, $C_{\rm ds}(V_{\rm ds}, V_{\rm gs})$, and $R_{\rm out}(V_{\rm ds}, V_{\rm gs})$. The RF equivalent circuit model is usually used for a device operated in the saturation region ($V_{\rm ds} > 1$ V). In addition, due to an increased channel leakage current at $V_{\rm ds} > 3$ V, which is associated with the short-channel effect, we limited the operation voltage below 3 V. Therefore, the results shown below were all obtained in this region, i.e., $1.0\ {\rm V} < V_{\rm ds} < 3.0$ V:

$$C_{\rm gs} = C_{\rm gs0}[1 + \tanh(\psi_1)][1 + \tanh(\psi_2)] \tag{3}$$

where

$$\begin{aligned} \psi_1 &= P_{\rm gs0} + P_{\rm gs1}V_{\rm gs} + P_{\rm gs2}V_{\rm gs}^2 + P_{\rm gs3}V_{\rm gs}^3 \\ \psi_2 &= Q_{\rm gs0} + Q_{\rm gs1}V_{\rm ds} + Q_{\rm gs2}V_{\rm ds}^2 + Q_{\rm gs3}V_{\rm ds}^3 \\ C_{\rm gd} &= C_{\rm gd0}[1 + \tanh(\psi_3)][1 - \tanh(\psi_4)] \end{aligned} \tag{4}$$

where

$$\begin{aligned} \psi_3 &= R_{\rm gd0} + R_{\rm gd1}V_{\rm gs} + R_{\rm gd2}V_{\rm gs}^2 + R_{\rm gd3}V_{\rm gs}^3 \\ \psi_4 &= S_{\rm gd0} + (S_{\rm gd1} + S_{\rm gd2}V_{\rm gs})V_{\rm ds} + S_{\rm gd3}V_{\rm ds}^2 + S_{\rm gd4}V_{\rm ds}^3 \\ C_{\rm ds} &= C_{\rm ds0}[1 - \tanh(\psi_5)] \end{aligned} \tag{5}$$

where

$$\begin{aligned} \psi_5 &= T_{\rm ds0}V_{\rm ds} + T_{\rm ds1}V_{\rm ds}^2 \\ R_{\rm out} &= R_{\rm out0}\frac{[1 + \tanh(\psi_6)]}{[1 - \tanh(\psi_7)]} \end{aligned} \tag{6}$$

where

$$\psi_6 = U_{\rm out0} + U_{\rm out1}V_{\rm gs} + U_{\rm out2}V_{\rm gs}^2 + U_{\rm out3}V_{\rm gs}^3$$

$$\psi_7 = V_{\rm out0} + (V_{\rm out1} + V_{\rm out2}V_{\rm gs})V_{\rm ds} + V_{\rm out3}V_{\rm ds}^2 + V_{\rm out4}V_{\rm ds}^3.$$

Fig. 5(a)–(c) shows the result for extracted and modeled $C_{\rm gs}$, $C_{\rm gd}$, and $C_{\rm ds}$, respectively. These nonlinear capacitances can be well modeled by the empirical equations shown previously. $C_{\rm gs}$, which is associated with the gate–oxide capacitance and the depletion region near source end, is mainly determined by $V_{\rm gs}$, and it is less $V_{\rm ds}$ dependent. $C_{\rm gd}$ has a strong dependence on $V_{\rm gs}$, which results from gate-to-drain bias conditions. At $V_{\rm gs} = 1.4$ V, $C_{\rm gd}$ is less dependent on $V_{\rm ds}$, which is due to the reversed p-n junction depletion at drain end. Under a higher $V_{\rm gs}$ bias condition, $C_{\rm gd}$ increases and is more dependent on $V_{\rm ds}$ due to a decrease of this depletion region. $C_{\rm ds}$ represents the drain-to-source substrate depletion effect, which is mainly determined by $V_{\rm ds}$, and it is less dependent

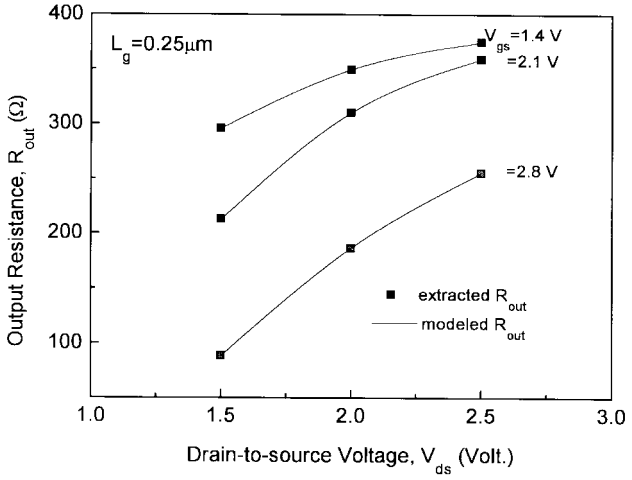

Fig. 6. Extracted and modeled bias dependent resistance $R_{\rm out}$, where $R_{\rm out0} = 256\ \Omega$, $U_{\rm out0} = 3.4$, $U_{\rm out1} = 0.69$, $U_{\rm out2} = -0.19$, $U_{\rm out3} = 0.41$, $V_{\rm out0} = -8.9$, $V_{\rm out1} = 1.0$, $V_{\rm out2} = 0.25$, $V_{\rm out3} = -4.2$, and $V_{\rm out4} = 0.58$ in (6).

on $V_{\rm gs}$. The variations of these bias-dependent capacitances are similar with the results obtained from [8], where the GaAs MESFET's were used. The only difference is that MESFET's are depletion-mode devices, and $C_{\rm ds}$ is strongly dependent on reversed $V_{\rm gs}$ bias, which is not the case in our MOSFET's.

The behavior of $R_{\rm out}$ (shown in Fig. 6) has a strong dependence on both $V_{\rm ds}$ and $V_{\rm gs}$. These changes are quite consistent with the results shown in Fig. 4, where the reciprocal of *I–V* slope is equivalent to $R_{\rm out}$. At a higher $V_{\rm gs}$ bias condition, a higher electric field causes a stronger short-channel effect, which results in a lower $R_{\rm out}$. Therefore, based on the results shown in Figs. 5 and 6, although these nonlinear elements were extracted from the S-parameters, the bias-dependent behaviors are qualitatively consistent with the physical predictions.

IV. Conclusion

In summary, for the first part of this paper, we characterized the dc and RF performance of deep-submicrometer MOSFET's. We observed the enhanced device performance by shrinking the gate length down to 0.25 μm. Based on the measured dc *I–V* and S-parameters, we constructed a nonlinear RF model for a 0.25-μm MOSFET. The empirical equations can fully model the behaviors of the nonlinear intrinsic elements. By combining nonlinear and bias-independent parasitics, an RF model for MOSFET is established for future circuit design of wireless communication.

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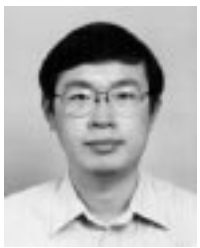

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